This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

Appl. No.: 10/066,376



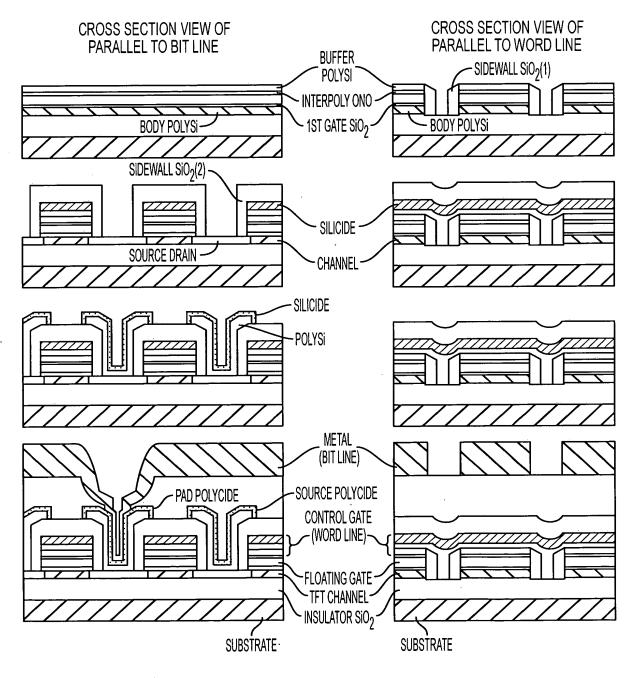


FIG. 1 PRIOR ART



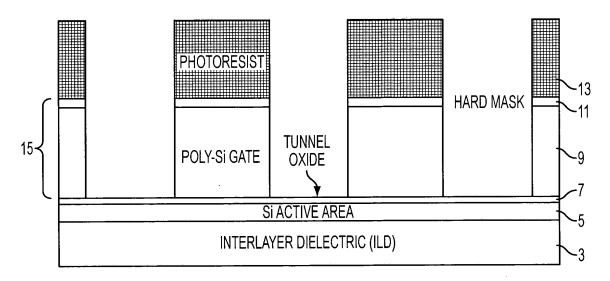


FIG. 2

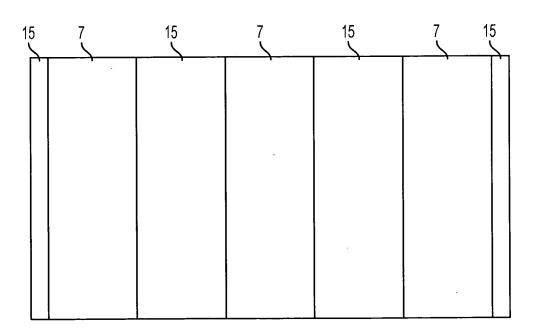


FIG. 3

Inventor(s): Igor G
Appl. No

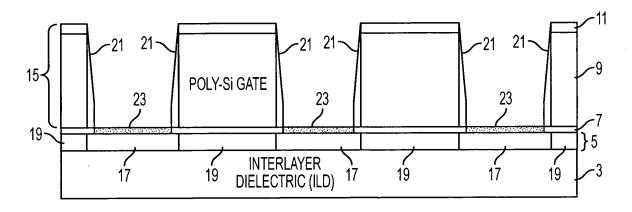


FIG. 4

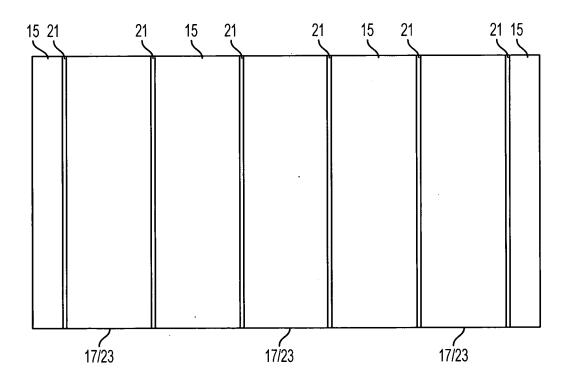


FIG. 5



FIG. 6

CIPE 16 THE MAY 1 & 2004 STATE OF

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING Inventor(s): Igor G. KOUZNETSOV et al. Appl. No.: 10/066,376

33 INTER-POLY DIELECTRIC **CONTROL GATE** -31 25 FLOATING GATE ISOLATION **OXIDE** BIT LINE CHANNEL CHANNEL **BIT LINE** }5 **BIT LINE** 23 19 INTERLAYER DIELECTRIC (ILD) A'**←**---

FIG. 7

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING

Inventor(s): Igor G. KOUZNETSOV et al. Appl. No.: 10/066,376



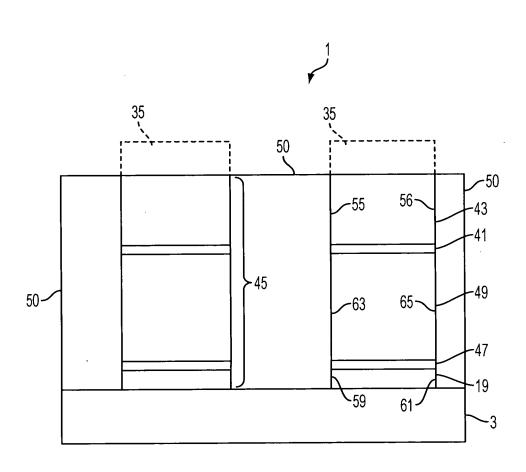


FIG. 8



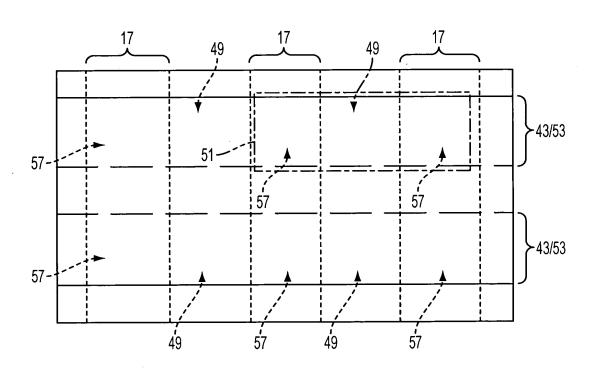


FIG. 9



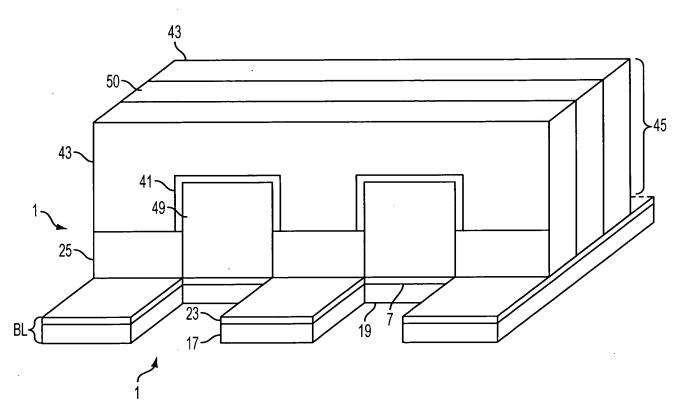
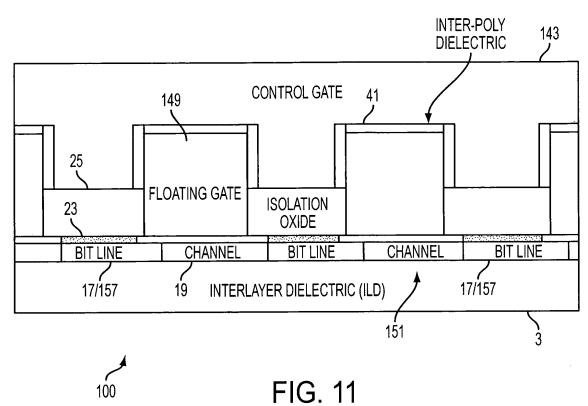
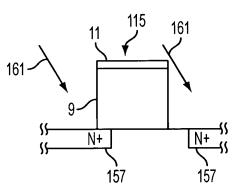


FIG. 10

Appl. No.: 10/066,376









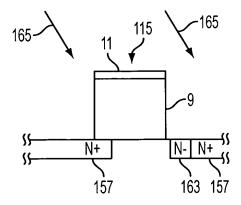


FIG. 13



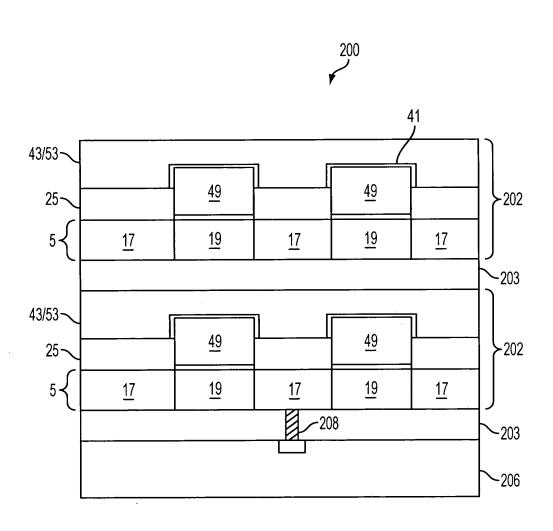


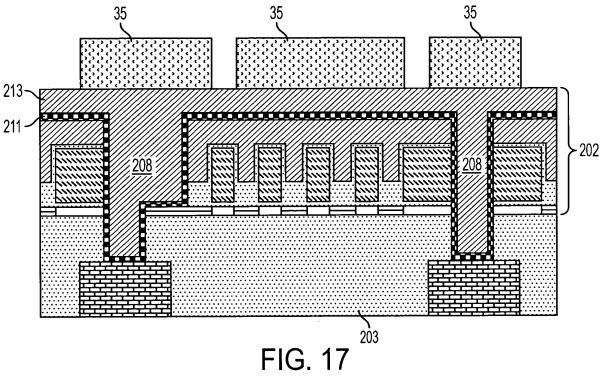
FIG. 14

Inventor(s): Igor G. KOUZNETSOV et al. Appl. No.: 10/066,376 209 209 209 33 31 - 202 19:::17:::19::17:::19: 203 202 202 or 206 or 206 FIG. 15 203

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING

FIG. 16





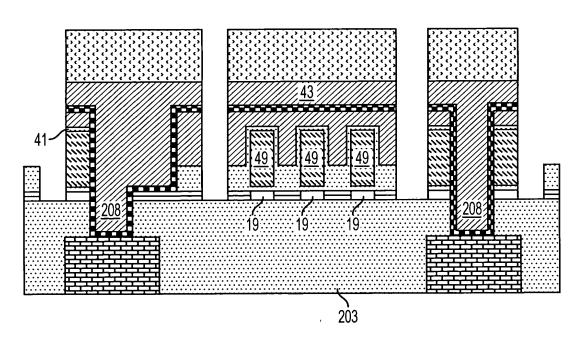


FIG. 18